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FORM PTO-1390 (REV. 11-94) **TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US)**	U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 10806-011 PCT 10/009552
INTERNATIONAL APPLICATION NO. PCT/SE00/00873	INTERNATIONAL FILING DATE May 4, 2000	PRIORITY DATE CLAIMED May 6, 1999
TITLE OF INVENTION SYNCHRONIZATION METHOD AND APPARATUS		
APPLICANT(S) FOR DO/EO/US Christer Bohm, Bengt J. Olsson, Magnus Danielson		

OIPE OCT 2 2 2001 PATENT & TRADEMARK OFFICE

Applicant herewith submits to the United States Designated/ Elected Office (DO/EO/US) the following items under 35 U.S.C. 371:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C 371(b) and PCT Articles 22 and 39(1).

4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the international Bureau).
   b. ☒ has been transmitted by the International Bureau
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b ☐ have been transmitted by the International Bureaus.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 37(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)) (not executed).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☐ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☐ Other items or information:

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INTERNATIONAL APPLICATION NO. PCT/SE00/00873	INTERNATIONAL FILING DA May 4, 2000	13 Rec'd PCT/PTO 22 OCT 2001

17. ☒ The U.S. National Fee (35 U.S.C. 371(c)(1)) and other fees as follows:

CLAIMS

(1)FOR	(2)NUMBER FILED	(3)NUMBER EXTRA	(4)RATE	(5)CALCULATIONS
TOTAL CLAIMS	20 -20	0	X $18.00	$ 0.00
INDEPENDENT CLAIMS	4 -3	1	X $84.00	84.00
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $280.00	$ 280.00
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☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) $710.00				
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a. ☐ A check in the amount of $___ to cover the above fees is enclosed.

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18. ☐ Other instructions
n/a

19. ☒ All correspondence for this application should be mailed to

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Garland Stephens	U.C. [illegible] Reg. No. 36,196 for Garland T. Stephens	37,242	10/22/01

SYNCHRONIZATION METHOD AND APPARATUS

Technical Field of Invention

The present invention refers to a method and an apparatus for synchronizing operation at a node of a communication network.

Background of the Invention

In all communication networks, an essential task to be addressed is how to synchronize the operation of the network and of the different equipment and components that form part of the network. Prior art provides many different approaches to address this task.

In most synchronous network systems, the operation of the entire network is strictly synchronized to a common synchronization source. In one example thereof, each node has its own direct connection to this common synchronization source, which is thereby connected to directly synchronize the operation at each node of the network. In another example, synchronization is forwarded from the common synchronization source through the network as such to reach all network nodes in a top-down manner, forming a so-called synchronization spanning-tree within the network. In the latter example, each output port of a node is typically strictly synchronized according to synchronization signals received at a currently designated input port of said node.

However, prior art schemes for distributing a frame frequency within a network while maintaining a high synchronization quality to reduce jitter are complicated and often require the use of expensive components and solutions while placing stringent requirements on the tow-down hierarchy, the network jitter, and/or negatively affecting data transport delays within the system.

The object of the invention is therefore to provide a simple and effective solution that provides a relaxed more flexible basis when defining synchronization trees

within a network and at the same time allows for optimization of the way in which synchronization is propagated at a node of the network.

Summary of the Invention

The above mentioned objects are achieved by the invention as defined in the accompanying claims.

According to an aspect of the invention, receiving two or more input frame synchronization signals are received at a node of the network, which in turn transmits an output frame synchronization signal, the output frame synchronization signal being associated with a predefined one of said input frame synchronization signals. For example, this association will typically be the association between an input port and an output port forming part of the same interface. A node common synchronization signal is then derived based upon a currently selected one of said input frame synchronization signals. The output frame synchronization signal is in turn generated using the node common frame synchronization signal as reference for synchronization. Moreover, a phase relationship between the output frame synchronization signal and the input frame synchronization signal that is associated therewith is determined. Based thereupon, said phase relationship is adjusted by the step of adjusting a phase relationship between the output frame synchronization signal and the node common synchronization signal when generating the output frame synchronization signal.

An advantage of the invention is that it makes it possible to design a network wherein the frame synchronization signal transmitted from an output port of a node is not synchronized strictly according to receptions of a frame synchronization signal received at the associated input port of the node, for example the input port forming part of the same interface as the output port. Instead, the frame synchronization signal transmitted

from the output port is primarily synchronized in relation to the occurrences of a node common synchronization signal, thereby gaining the quality of the node common synchronization signal, and indirectly according to the receptions of the frame synchronization signal received at the associated input port, thereby to adjust the delay with respect to the input port.

This means that if the node for example is connected to a unidirectional communication bus, said input port being connected to receive frames of data from said bus and said output port being connected to transmit frames of data to said bus, the transmission of frames from the output port need not be strictly synchronized to the reception of frames at the input port. The output port may instead be synchronized according to a frame signal that, for example, is received at another port of the node (typically nominally having the same frame frequency as the one on said input port, or a multiple thereof), but then in such a way that the phase relationship between the reception of frames from the input port and the transmission of frames from the output port is taken into consideration. In other words, when the input port and the output port together form an interface to a unidirectional bus, the synchronization signal that is used to synchronize the operation at the output port need not be the synchronization signal that is received from the unidirectional link that is received at said input port. As a consequence, the actual "time-keeper" on a bus need not be a head end node on the bus, or, in broader terms, the actual frame synchronization tree need not strictly coincide with a data transport tree. This consequently has the advantage of allowing a greater freedom and flexibility when defining and building a synchronization tree of the above-mentioned kind for propagating synchronization signals through a communication network.

Another advantage of the invention is that is makes it possible to control the delay through the node in a

very simple and flexible way. For example, when a node is connected to a unidirectional communication bus in the above-mentioned manner, it generally preferred that the delay, i.e. the time period between the point in time when a time slot of data is received at the input port and when it is transmitted from the output port, is as low as possible. In other words, it is preferred that frames of data received at said input port is transmitted as soon as possible from the output port. This would imply that the difference in time between the reception of an input frame synchronization signal and the transmission of an output frame synchronization signal should be as low as possible. However, a low delay typically implies the use of very low fill levels in buffers that are typically used at said ports for temporarily storing said data. Consequently, if a small fluctuation in synchronization rates or in data forwarding mechanisms occurs, there is a risk that said buffers will run empty, which may have the effect that there is no valid data available for transmission when transmission is due. Therefore, a certain level of buffering is preferred. Consequently, the difference in time between the reception of the input frame synchronization signal and the transmission of the output frame synchronization signal should not be too low. Whether needed as a result of these or other considerations, the invention provides a very simple solution for controlling the delay as desired.

This feature is also very advantageous when a plurality of nodes are connected to a unidirectional bus that forms a single ring or loop with one node acting as head as well as terminating end of the loop. When closing the loop, the point in time at which the head end node transmits the start of a frame as head-end will typically not coincide with the point in time that it receives the start of a frame as terminating-end. If this difference in time should, for example, correspond to half a frame, then half a frame of data would have to be buffered at

the head end node. This could for example mean a communication channel that is set up over a portion of the ring that includes the head-end node would show a large delay as compared to a communication channel that is set up over a portion of the ring that does not include the head-end node. However, by controlling the delay at the different nodes connected to the loop, in accordance with the invention, the required buffering needed to accommodate for the half-frame difference created by the closing of the loop may be distributed among all nodes of the ring in any desired way. If the required buffering for example were distributed evenly among all nodes of the ring, a communication channel established over the ring will show the same delay irrespective of which portion of the ring that is established over. The delay would of course then still be a function of the number of nodes that the channel passes on the ring.

As an alternative to the latter situation, if the situation is such that a majority of the communication channels that are established over the ring is done so over a specific portion of the ring, it may be desirable to keep the buffering, and consequently, the delay over this portion of the ring to a minimum. It would then be preferred to redistribute the buffering that is required as a result of the closing of the ring to a portion of the ring over which only a minority of the communication channels are established.

To be understood, the node synchronization signal may for example be generated using another input frame synchronization signal received at an input port of the node, a synchronization signal generated locally at said node, or even another output frame synchronization signal transmitted from another port of the node, as reference. The node synchronization signal may in fact itself be another input frame synchronization signal, a synchronization signal generated locally at said node, or another

output frame synchronization signal transmitted from another port of the node.

However, according to a preferred embodiment, said node synchronization is generated using a signal of two or more input frame synchronization signals as reference. Furthermore, it is preferred that said node synchronization signal is generated in such a way that a change of input frame synchronization signal to be used as said reference does not cause any phase shifts in said node synchronization signal. The latter may for example be accomplished by the step of determining the frame phase difference between said node synchronization signal and one of said input frame synchronization signals that is to be used as said reference and to change into using this signal as reference in such a way that the determined frame phase difference is maintained. As this feature has the advantage of not causing any phase-shifts in the node synchronization signal, and as the node synchronization signal is used as reference for transmitting said output frame synchronization signal, a phase-shift free behavior of the output frame synchronization signal is ensured when a switch of synchronization source is required. For definition, a phase-shift herein refers to the situation wherein an essential discontinuity, or "jump", occurs or is generated in the phase of a signal.

According to an embodiment of the invention, output frame synchronization signals transmitted from two or more output ports of said node are controlled to show a respective phase difference in relation to said node synchronization signal, the respective phase differences being permissible to be adjusted individually for each respective output port. This embodiment has the advantage of allowing for different phase situations to exist simultaneously at different output ports of the node.

The invention is especially advantageous in networks wherein the synchronization requirements are such that each frame synchronization signal may show a limited

jitter and may be arbitrarily located in phase in relation to other frame synchronization signals, but may not show any persistent frame drift in relation to other frame synchronization signals. For example, the maximum allowable jitter may be 1000 ppm and the maximum allowable frame drift may be one (1) frame.

Specifically, the invention is contemplated for use in a DTM-network (Dynamic synchronous Transfer Mode) wherein the synchronous multi-topology network are provided with mesochronous properties to provide for simpler design and architectural freedom of the network as well as the network nodes. Further information on the basics of DTM technology is found in "The DTM Gigabit Network", Christer Bohm, Per Lindgren, Lars Ramfelt, and Peter Sjödin, Journal of High Speed Networks, 3(2):109-126, 1994, and "Multi-gigabit networking based on DTM", Lars Gauffin, Lars Håkansson, and Björn Pehrson, Computer networks and ISDN Systems, 24(2):119-139, April 1992.

As noted, the invention is primarily conserned with the propagation of synchronization on a frame level. To be understood means for providing synchronization on a bit or slot level, while synchronizing a bit frequency and/or a slot frequency, could be added as well. However, note that for example in the DTM network, a nominal bit frequency will be generated individually by each node for and will thus essentially not be propagated through the network.

This application is one in a series of three applications that were filed at the Swedish Patent Office on the same day, having the same title, the same applicant, and all referring to related inventive ideas, the description of the other two hereby being incorporated herein by reference.

The above mentioned and other aspects, features and details of the invention will be more fully understood from the following description of a preferred embodiment thereof.

Brief Description of the Drawings

Exemplifying embodiments of the invention will now be described with reference to the accompanying drawings, wherein:

Fig. 1 schematically shows a DTM network;

Fig. 2 schematically shows an exemplifying design of a network node according to an embodiment of the invention;

Fig 3 schematically show an embodiment of the node synchronization block shown in Fig. 2;

Fig. 4 schematically shows characteristics of the generator of the node synchronization block illustrated in Fig. 3; and

Figs. 5A and 5B schematically show two different embodiments of the invention exemplifying implementations the output port blocks shown in Fig. 2.

Detailed Description of Preferred Embodiments

Fig. 1 schematically shows a DTM network 110 comprising nine nodes 111-119 that are interconnected via unidirectional network links, for example in the form of optical fibers, illustrated as arrows. For example, node 111 is connected directly to node 112 via two unidirectional links (one output link connected to transport signals to node 112 and one input link connected to transport signals in the opposite direction, i.e. from node 112). Similarily, node 113 is connected to node 112 via two unidirectional links (one output link transporting signals to node 112 and one input link transporting signals from node 112), to node 114 via two unidirectional links (one output link transporting signals to node 114 and one input link transporting signals from node 114), to node 116 via one unidirectional output link transporting signals to node 116, and to node 119 via one unidirectional input link transporting signals from node 119.

In Fig. 1, the links that interconnect nodes 111-115 may each be configured as a point-to-point link. However, more preferably, nodes 111-115 will be configured to regard these links as together forming a bi-directional, multi-access double bus. Similarly, nodes 113, 116, 117, 118, and 119 will typically be configured to regard the links that interconnect nodes 113, 116, 117, 118, and 119 as together forming a unidirectional, multi-access single ring bus.

The network 110 also comprises two external clock reference sources 121 and 122, such as atomic or GPS clocks, connected to node 111 and node 118, respectively. In addition, each one of the nodes 111-119 comprises a respective internal clock reference source (not shown). To make sure that there is only one reference source that is used as synchronization master with in the network at each point in time, each reference source is assigned a so-called reference source priority.

In the exemplifying network, in order to establish synchronization within the network 110, each node 111-119 is arranged to transmit so called synchronization messages to its neighbors, more specifically to neighbors that it has an output link to, and will receive similar synchronization messages from neighbors that it has a input link from. Each message will contain information related to the quality of synchronization available at the node transmitting the message. Based upon such synchronization information received in such messages, each node will select which node, or rather which input link, to use as its reference for synchronization, i.e. to use as synchronization source, as will be described more in detail below.

Fig. 2 schematically shows a network node 200 that comprises three input port blocks 250a-250c, a node synchronization block 300, a switch core 400, a node controller 450, and three output port blocks 500a-500c.

Each one of the input port blocks 250a-250c is arranged to receive regularly occurring frames of data, divided into time slots, from respective input links. The location of each frame on the respective link is identified by an input frame synchronization signal, also being referred to as a frame start signal while being located in the stream of data to mark the beginning of each frame, which is carried along with the frames on the respective link. In this example, it is assumed that the frame frequency is nominally 8 kHz, corresponding to a frame length of 125 μs. Consequently, the frame synchronization signal of each respective link will be nominally received each 125 μs at the respective input port block.

Each input port block 250a-250c is arranged to derive data from time slots of received frames and to transmit such slot data to the switch core 400. Also, each input port block 250a-250c is arranged to derive the respective input frame synchronization signal from the respective input stream of data and to transmit said signal to the node synchronization block 300 and to a respective output port block 500a-500c.

The switch core 400 is arranged to switch slots of data from the input port blocks 250a-250c to the output port blocks 500a-500c in accordance with switching instructions defined by the node controller 450. Furthermore, the switch core 400 is arranged to switch slots of data received in one or more control channels at the input port blocks 250a-250c from the input port blocks 250a-250c to the node controller 450, and to switch time slots of data to be transmitted in one or more control channels at the output port blocks 500a-500c from the node controller 450 to the output port blocks 500a-500c.

Data received/transmitted in said control channels from/to other nodes of the network will typically include channel management information. Based upon such channel management information, the node controller 450 will

provide the switch core 400 with said switching instructions.

Data received/transmitted in said control channels will also include synchronization messages of the kind discussed above with reference to Fig 1. Based upon an evaluation of such synchronization messages, the node controller 450 will select which input link, i.e. which input frame synchronization signal, that is to be used as synchronization source for synchronizing of the operation of the node 200. Based upon such a selection, the node controller 450 is connected to provide the node synchronization block 300 with a synchronization selection signal that identifies which input frame synchronization signal to use as synchronization source, the timing at which a switch to using another frame synchronization signal as synchronization source is to take place, and similar related information.

The node synchronization block 300 is connected to receive the input frame synchronization signals from the respective input port blocks 250a-250c and the synchronization selection signal from the node controller 450. Based upon these signals, the node synchronization block 300 is arranged to generate a node internal frame synchronization signal, also referred to below as node synchronization signal. The node synchronization signal is generated to have a continuous phase, i.e. to be essentially phase-shift free, which means that a change of synchronization source for generating said node synchronization signal will not cause any essential discontinuities or phase-shifts in the node synchronization signal. The node synchronization signal generated by the node synchronization block is transmitted to each one of the output port blocks 500a-500c. Examples on how the phase-shift free node synchronization signal is generated by the node synchronization block 300 will be described in detail below with reference to Figs. 3A and 3B.

Each one of the output port blocks 500a-500c typically receives data in slots from the switch core 400, input frame synchronization signals from a respective input port block 250a-250c, and the node synchronization signal from the node synchronization block 300. Using the node synchronization signal as synchronization source, optionally taking into account the phase of the respective received input frame synchronization signal, each output port will generate a respective output frame synchronization signal and will transmit said output frame synchronization signal as a frame start signal along with frames of time slot data received from the switch core 400 on a respective output link. Examples on how this is performed will be described in detail below with reference to Figs. 5A and 5B.

In operation, input port block 250a and output port block 500a could typically be configured as together forming a first input/output interface, input port block 250b and output port block 500b would be configured as together forming a second input/output interface, and input port block 250c and output port block 500c, would be configured as together forming a third input/output interface. Each interface would then optionally be connected to provide read and write access to a respective unidirectional bus, wherein frames of slots received at, for example, the input port 250a would be switched essentially as a whole by the switch core 400 to be transmitted essentially unaffected, with the exemption of specific slots being switch to/from other ports, at output port 500a. As an example, if node 200 would be configured as node 113 in Fig. 1, said first interface would be connected to provide access to the unidirectional bus from node 111 to node 115. More specifically, input port block 250a would be connected to the link from node 112 and output port block 500a would be connected to the link to node 114. Similarly, said second interface would be connected to provide access to the uni-

directional bus from node 115 to node 111, and said third interface would be connected to provide access to the unidirectional single ring bus.

An embodiment 300 exemplifying an implementation the node synchronization block 300 shown in Fig. 2 will now be described with reference to Fig. 3. The embodiment 300 comprises a selection unit 343, a phase offset detector 313, a first sample-and-hold circuit 323, a subtracting circuit 324, a low-pass filter 325, an adding circuit 326, a second sample-and-hold circuit 327, and a node synchronization signal generator 348.

As illustrated in Fig. 3, the block 300 is connected to receive input frame synchronization signals from all input port blocks 250a-250c. The block 300 is moreover arranged to generate a phase-shift free node synchronization signal based thereupon as controlled by control signals from the node controller 450, and to output said node synchronization signal to the output port blocks 500a-500c.

For that purpose, the selection unit 343 is connected to receive the input frame synchronization signals from the three input port blocks 250a-250c, and to forward signals from one of these three input port blocks, as selected by the control signal from the node controller 450, to the phase offset detector 313.

The detector 313 is connected to receive the input frame synchronization signal from the selection unit 343 as well as a feedback copy of the node synchronization signal that is outputted from the generator 348. The detector 313 will determine the phase offset between the node synchronization signal and the input frame synchronization signal, said offset being outputted as an offset value to the first sample-and-hold circuit 323 and to the subtracting circuit 324.

The first sample-and-hold circuit 323 is in turn connected to sample the offset value from the detector 313 and to output a fixed offset value to the subtracting

circuit 324. The sampled offset value is used to update the outputted fixed offset value at timings determined by the control signal from the node controller 450.

The subtracting circuit 324 is arranged to subtract the fixed offset value, outputted by the first sample-and-hold circuit 323, from the offset value outputted by the detector 313, and to output a resulting offset deviation to the low-pass filter 325, which in turn outputs a low-pass filtered deviation to the adding circuit 326.

The adding circuit 326 is arranged to add the low-pass filtered deviation, as outputted by the low-pass filter 325, to the output from the second sample-and-hold circuit 327, and to output the thus resulting modified deviation as a frequency control signal to the generator 348 and to the second sample-and-hold circuit 327. The second sample-and-hold circuit 327 is furthermore arranged to sample said modified deviation and to update its fixed output at timings determined by control signals from the node controller 450.

The generator 348 is arranged to generate said node synchronization signal, having a frequency of approximately 8 kHz, as a function of the received control signal. More specifically, the generator 348 in this example has the characteristics illustrated in the diagram of Fig. 4. As shown in Fig. 4, if the received frequency control signal is zero (0), the frequency of the outputted node synchronization signal will be approximately 8000 Hz. However, if the received frequency control signal increases to, lets say, two (2), the frequency of the outputted node synchronization signal will increase to approximately 8001 Hz. Similarly, if the received frequency control signal decreases to, lets say, minus two (-2), the frequency of the outputted node synchronization signal will decrease to approximately 7999 Hz.

The embodiment illustrated in Fig. 3 forms a feed-back loop that continuously strives to bring the offset

detected by the detector 313 to be equal to the fixed, "desired" offset output from the first sample-and-hold circuit 323 by the continuous adjustment of the output frame frequency of the generator 348. Any deviation between the offset from the detector 313 and the offset from the hold-over-circuit 323 will result in a non-zero input to the low-pass filter. If such a deviation is persistent over time, it will eventually be forwarded via the low pass filter 325 and the adding circuit 326 to the generator 348, and will then cause a small change in the frequency of the outputted node synchronization signal. This small change in frequency will act to slowly bring said difference back to zero.

To be noted, in a steady state situation, the frequency control signal inputted to the generator 348 will reflect the frequency of the input synchronization signal that is currently forwarded by the selection unit 343. Consequently, at repeated intervals, the node controller 450 will instruct the second sample-and-hold circuit 327 to incrementally/decrementally update its output in accordance with the current output from the adding circuit 326. This updating of the output of the second sample-and-hold circuit 327 provides a means for "memorizing" the network frequency. Note however that such updatings are in this exemplified embodiment performed in small steps in order to not give rise to any sudden large changes in the frequency control signal input to the generator 348.

In Fig. 3, when a change of synchronization source is to take place, the node controller will instruct the selection unit 343 to forward another input synchronization signal to the detector 313. As soon as the offset between the new input synchronization signal and the node synchronization signal has been determined and outputted by the detector 313, the node controller 450 will instruct the first sample-and-hold circuit 323 to update its output with to this new offset. The new offset is

thereby set as the new desired offset that the design will strive to maintain in relation to the new input synchronization signal. As is understood, the normalization of the offset, as performed by the subtracting unit 324, in conjunction with the use of the low-pass filter 325, provides for a smooth behavior of the node synchronization signal generated by the generator 348 when switching synchronization source.

An embodiment 500-A exemplifying an implementation of an output port block of the kind denoted 500a-500c in Fig. 2 will now be described with reference to Fig. 5A. The embodiment 500-A comprises a frame buffer 510, an output port 520, a phase offset detector 530, a phase offset control unit 540, and a phase offset generator 550.

As described above with reference to Fig. 2, and as illustrated in Fig. 5A, the block 500-A is connected to receive time slot data from the switch core 400, an input frame synchronization signal from a respective one of the input port blocks 250a-250c, a phase control signal (not shown in Fig. 2) from the node controller 450, and the node synchronization signal from block 300. Based upon the inputs, the block 500-A is arranged to output frames.

For that purpose, the frame buffer 510 is connected to receive said time slot data from the switch core and to store said time slot data prior to the transmission thereof from the output port 520. The output port 520 is in turn arranged to receive an output frame synchronization signal from the phase offset generator 550 and to transmit 125 μs frames of time slot data, as provided by the frame buffer, using said output frame synchronization signal to synchronize the transmission of the start of each frame.

The phase offset detector 530 is connected to receive the input frame synchronization signal from the respective one of the input port blocks 250a-250c, as

well as a feedback copy of the output frame synchronization signal from the phase offset generator 550.

The detector 530 is arranged to determine the phase difference, i.e. phase offset, between the input frame synchronization signal and the output frame synchronization signal. The detector 530 is implemented as a counter that is reset and started at the reception of each input frame synchronization signal and that is stopped at the reception of each output frame synchronization signal, counting at a rate of approximately 1000 counts per 125 μs. Each so determined offset, provided as an offset count in the interval of 0 to approximately 1000, is then outputted to the phase offset control unit 540.

As illustrated in Fig. 5A, the phase offset control unit 540 is connected to receive the phase offset count from the detector 530, as well as the phase offset control signal from the node controller 450. As the phase offset count represents the difference in time between the input frame synchronization signal and the output frame synchronization signal, it also will reflect the overall delay through the node in Fig. 2, i.e. the time that it takes for data to pass through the switch from the input port providing the input frame synchronization signal to the output port 520. The purpose of the control unit 540 is to compare the offset count received from the detector 530 with a selected offset count, representing a desired delay through the node, received as said phase offset control signal from the node controller 450. Based upon such a comparison, the control unit 540, typically implemented in software, will generate an output offset count that is outputted to the phase offset generator 550. Typically, if the offset count received from the detector 530 is smaller than the selected offset indicated by the control signal from the node controller 450, i.e. if the delay through the node is smaller than desired, the control unit 540 will increment the offset count outputted to the generator 550. On the other hand, if the

offset count received from the detector 530 is higher than the selected offset indicated by the control signal from the node controller 450, i.e. if the delay through the node is larger than desired, the control unit 540 will decrement the offset count outputted to the generator 550.

The phase offset generator 550 is arranged to receive the node synchronization signal from block 300 and to add the offset received from the control unit 540 thereto, thereby adjusting the phase of the frame synchronization signal outputted from the generator 550 to provide for a desired delay through the node. In this example, the generator 550 is implemented as a counter that is reset and started at the reception of the node synchronization signal and that transmits the phase adjusted output frame synchronization signal at the point in time that the counter reaches the count defined by the offset count input from the control unit 540, counting at said rate of approximately 1000 counts per 125 μs. As another example, a generator of the kind described with reference to Fig. 3 could be used.

The so phase-adjusted output frame synchronization signal from the generator 550 is then fed to the detector 530 and to the output port 520, which will transmit frames of data based thereupon as described above.

Consequently, the function of the detector 530, the control unit 540, and the offset generator 550 is to adjust the transmission of the output frame synchronization signal to provide for a desired delay through the node. Furthermore, as the output frame synchronization signal is generated using the node synchronization signal as reference, the latter having been generated as described above to be essentially phase shift free irrespective of any change of input frame synchronization signal to be used as synchronization source, an essentially continuous behavior of the output frame synchronization signal is ensured.

Another embodiment 500-B exemplifying an implementation an output port block of the kind denoted 500a-500c in Fig. 2 will now be described with reference to Fig. 5B. The embodiment 500-B comprises a frame buffer 511, an output port 521, a buffer fill level detector 531, a phase offset control unit 541, and a phase offset generator 550.

The operation and function of the buffer 511, the output port 521 and the offset generator 551 are essentially the same as those of the buffer 510, the output port 520 and the offset generator 550 described with reference to Fig. 5A, and further detailed description thereof is therefore omitted in the following.

The block 500-B in Fig. 5B differs from the block 500-A in Fig. 5A in that it is not connected to receive the input frame synchronization signal from one of the input port blocks 250a-250c in Fig. 2. Instead, the block 500-B comprises the buffer fill level detector 531 which is arranged to repeatedly determine the fill level of the buffer 511, i.e. to monitor the amount of time slot data that is stored in the frame buffer, and to provide a measure of the fill level to the control unit 541. As the amount of time slot data stored in the frame buffer will depend upon the overall delay through the node, said buffer fill level is compared in the control unit 541 against a desired buffer fill level that is designated by the control signal from the node controller 450. The control unit will then increment or decrement its phase offset count output to the phase offset generator 551 based upon this comparison. Typically, if the measured buffer fill level is smaller than the selected fill level indicated by the control signal from the node controller 450, typically corresponding to a smaller delay than desired, the control unit 541 will increment the offset count outputted to the generator 551. On the other hand, if the determined buffer fill level is higher than the desired fill level indicated by the control signal from

the node controller 450, typically corresponding to a higher delay than desired, the control unit 541 will decrement the offset count outputted to the generator 551.

Consequently, the block 500-B uses the buffer fill level of the buffer 511 as a measure of the delay, and adjusts the transmission of the output frame synchronization signal accordingly. With this exemption, the operation of the block 500-B is essentially the same as the one of the block 500-A described above with reference to Fig. 5A.

Even though exemplifying embodiments of the invention have been described in detail above with reference to the accompanying drawings, different modifications, combinations and alterations thereof may be made within the scope of the invention, which is defined by the accompanying claims.

CLAIMS

1. A method for synchronizing operation at a node of a communication network, said method comprising:

receiving two or more input frame synchronization signals and transmitting an output frame synchronization signal, the output frame synchronization signal being associated with a predefined one of said input frame synchronization signals;

selecting one of said input frame synchronization signals to define a node common frame synchronization signal;

generating the output frame synchronization signal using the node common frame synchronization signal as reference for synchronization;

determining a phase relationship between the output frame synchronization signal and the input frame synchronization signal that is associated therewith; and, based thereupon

adjusting said phase relationship by adjusting a phase relationship between the output frame synchronization signal and the node common synchronization signal when generating the output frame synchronization signal.

2. A method as claimed in claim 1, wherein said adjusting step is performed with the purpose of controlling the time difference between each transmission of the output frame synchronization signal each reception of the input frame synchronization signal that is associated therewith.

3. A method as claimed in claim 2, wherein said adjusting step comprises increasing said phase difference if said time difference is smaller than a selected time difference, and decreasing said phase difference if said time difference is larger than said selected time difference.

4. A method as claimed in claim 1, 2, or 3, wherein data to be outputted as part of frames defined by said output frame synchronization signal is stored in a memory prior to transmission thereof, the data fill level of said memory reflecting the phase relationship between the output frame synchronization signal and the input frame synchronization signal that is associated therewith, and wherein the phase relationship between the output frame synchronization signal and the node common synchronization signal is adjusted so as to maintain a selected data fill level of said memory.

5. A method as claimed in any one of the preceding claims, wherein frames defined by said frame synchronization signals occur regularly, are of fixed size, and are each divided into a plurality of fixed sized time slots.

6. A method as claimed in any one of the preceding claims, comprising:

transmitting, in addition to said output frame synchronization signal, at least one other output frame synchronization signal, each output frame synchronization signal being generated using said node common synchronization signal as reference for synchronization; and

adjusting each output frame synchronization signal individually to show a respective phase relationship in relation to said node common synchronization.

7. A method as claimed in claim 6, each output frame synchronization signal being associated with a respective input frame synchronization signal, said method comprising adjusting a respective phase relationship between each respective output frame synchronization signal and the respective associated input frame synchronization signal by adjusting the respective phase relation-

ship between each respective output frame synchronization signal and the node common frame synchronization signal.

8. A method as claimed in any one of the preceding claims, comprising defining said node common frame synchronization signal in such a way that a change in the selection of input frame synchronization signal to define said node common synchronization signal does not cause any phase shifts in said node common synchronization signal.

9. A method as claimed in claim 8, comprising determining the frame phase difference between the node common synchronization signal and at least one of said input frame synchronization signals that is to define said node common synchronization signal, wherein a change into using said input frame synchronization signal to define said node common synchronization signal is performed in such a way that the determined frame phase difference between said node synchronization signal and said input frame synchronization signal is maintained.

10. A method as claimed in any one of the preceding claims, wherein said output frame synchronization signal is to be synchronized in relation to an input frame synchronization signal in such a way that:

a) said output frame synchronization signal is permitted to show an arbitrary phase difference in relation to said input frame synchronization signal;

b) said output frame synchronization signal is permitted to show an acceptable phase jitter in relation to said input frame synchronization signal; and

c) said output frame synchronization signal is not permitted to show any persistent phase drift in relation to said input frame synchronization signal.

11. A method as claimed in any one of the preceding claims, wherein said method is performed in a time division multiplexed circuit switched network.

12. A method as claimed in any one of the preceding claims, wherein each one of said frame synchronization signals is an in-band frame start signal that is transmitted on a respective link to designate the start of each frame transmitted thereon.

13. A method for synchronizing operation at a node of a communication network, comprising:

receiving an input frame synchronization signal;

transmitting an output frame synchronization signal that is associated with said input frame synchronization signal;

controlling a phase relationship between the output frame synchronization signal and the input frame synchronization signal by the step of adjusting a phase relationship between the output frame synchronization signal and signal that is defined optionally using another input frame synchonization signal as reference for synchronization.

14. An apparatus in a communication network, said apparatus comprising:

an interface defined by input means (250) for recieving an input frame synchronization signal and associated output means (500) for transmitting an assiciated output frame synchronization signal;

means (300) for providing a node common synchronization signal derived from a currently selected one of two or more input frame synchronization signals, one thereof being the first mentioned input frame synchronization signal;

means (530; 531) for determining a phase relationship between the first mentioned input frame synchroniza-

tion signal and the associated output frame synchronization signal;

means (540, 550; 541, 551) for generating said output frame synchronization signal using said node common synchronization signal as reference and, in doing so, adjusting the phase relationship between the first mentioned input frame synchronization signal and the output frame synchronization signal as desired by adjusting a phase relationship between the node common synchronization signal and the output frame synchronization signal.

15. An apparatus as claimed in claim 14, comprising means (530, 540, 550; 531, 541, 551) for generating another output frame synchronization signal using said node common synchronization signal as reference and, in doing so, adjusting a phase relationship between said another output frame synchronization signal and a respective input frame synchronization signal associated therewith by adjusting a phase difference between said another output frame synchronization signal and the node common synchronization signal.

16. An apparatus as claimed in claim 15, comprising means (450, 540; 450, 541) for adjusting said phase differences of said output frame synchronization signals in relation to said node synchronization signal so that each one of said output frame synchronization signals is controlled to show a respective phase difference in relation to said node synchronization signal, said respective phase difference being controlled individually for each respective output frame synchronization signal.

17. An apparatus as claimed in any one of claims 14, 15, or 16, said means (300) for providing a node common synchronization signal being arranged to derive said node common synchronization signal in such a way that a change

of input frame synchronization signal to be used to derive the node common synchronization signal does not cause any phase shifts in said node common synchronization signal.

18. An apparatus as claimed in any one of claims 14-17, said apparatus being arranged to synchronize said output frame synchronization signal in relation an input frame synchronization signal in such a way that:

a) said output frame synchronization signal is permitted to show an arbitrary phase difference in relation to said input frame synchronization signal;

b) said output frame synchronization signal is permitted to show a limited phase jitter in relation to said input frame synchronization signal; and

c) said output frame synchronization signal is not permitted to show any persistent phase drift in relation to said input frame synchronization signal.

19. An apparatus as claimed in any one of claims 14-18, wherein said apparatus is operating in a time division multiplexed circuit switched network.

20. An apparatus in a communication network, comprising:

an interface comprising an input port for receiving an input frame synchronization signal and an output port for transmitting an output frame synchronization signal; and

means being arranged to control a phase relationship between the output frame synchronization signal and the input frame synchronization signal by adjusting a phase relationship between the output frame synchronization signal and a reference signal that as such is defined optionally using another input frame synchonization signal as reference for synchronization.

1/5

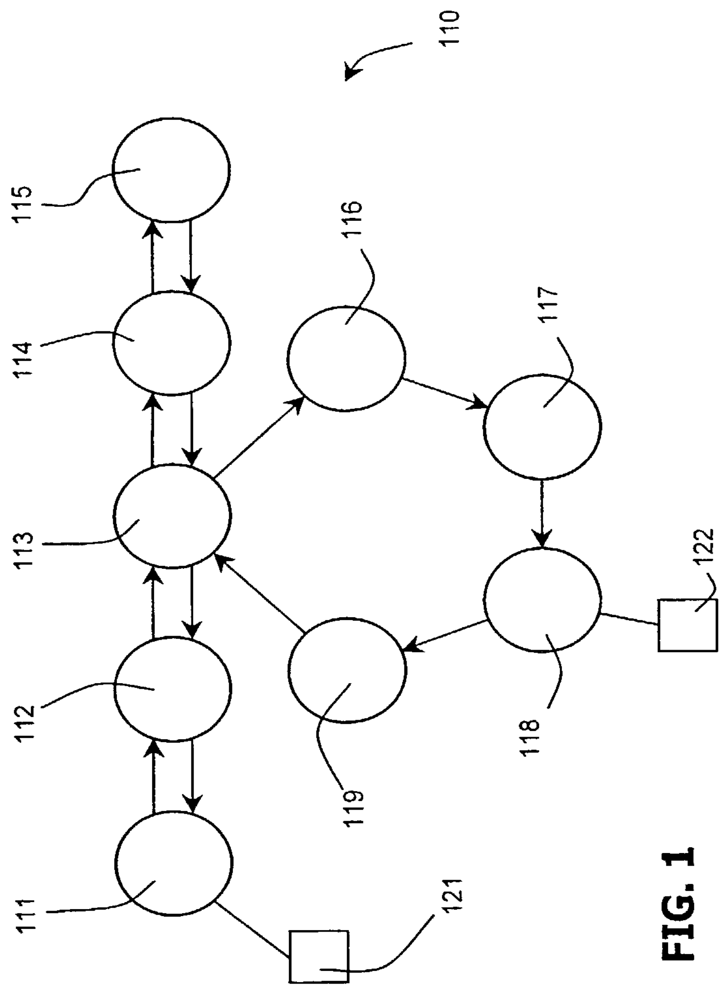


FIG. 1

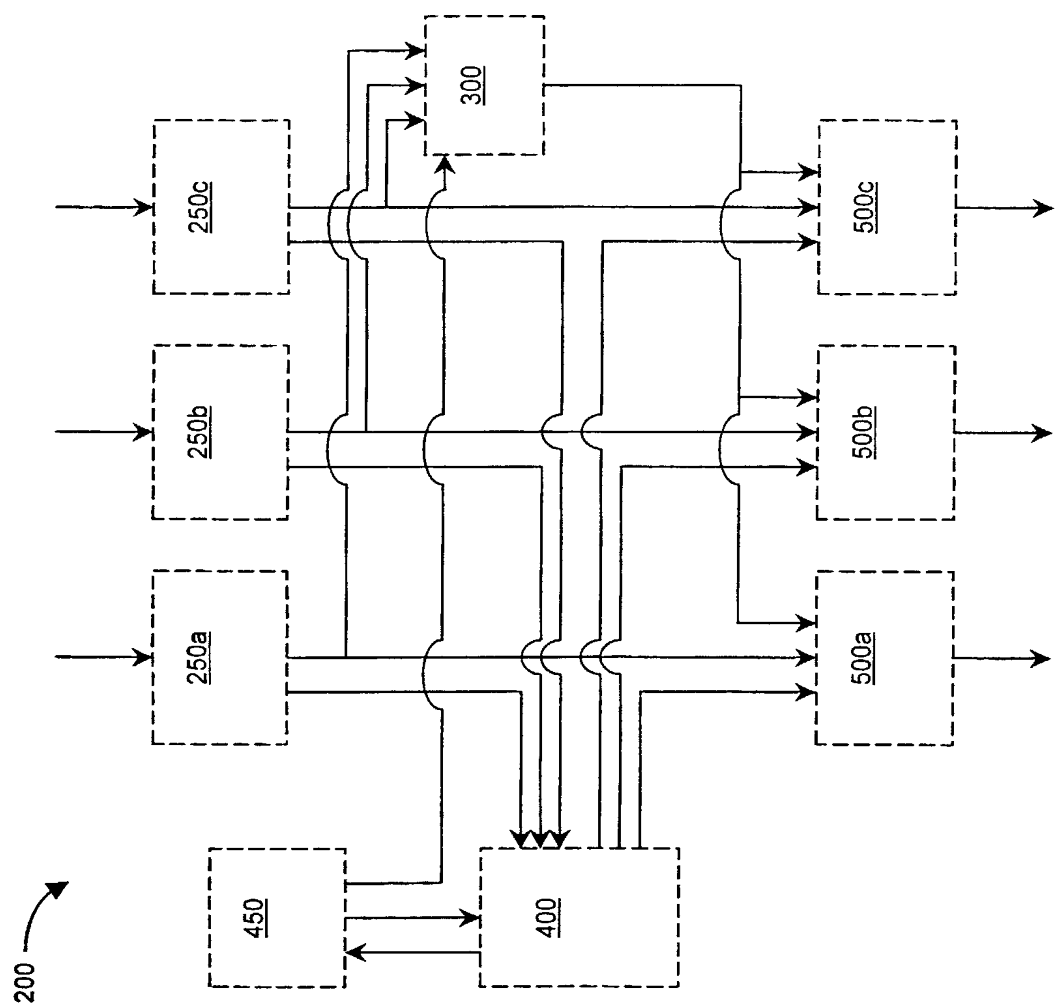


FIG. 2

10/009552

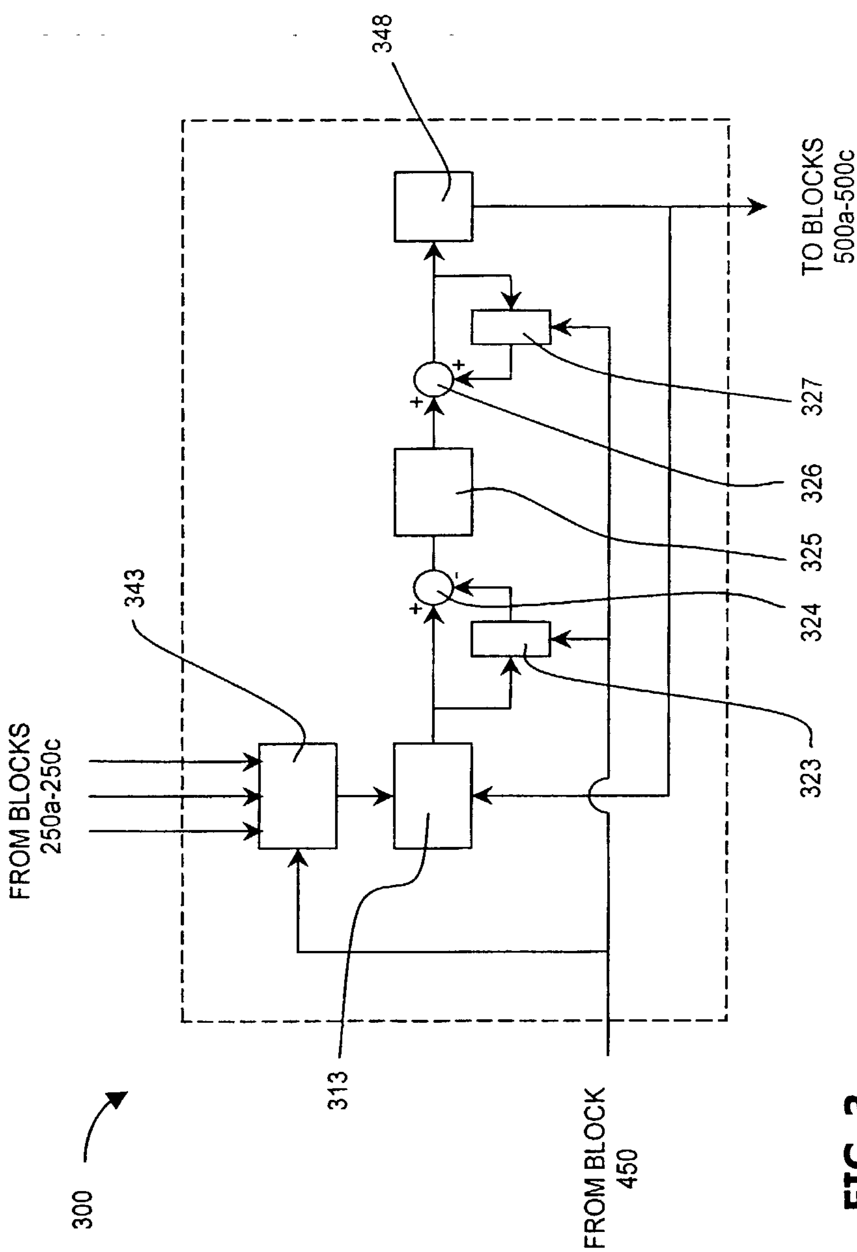


FIG. 3

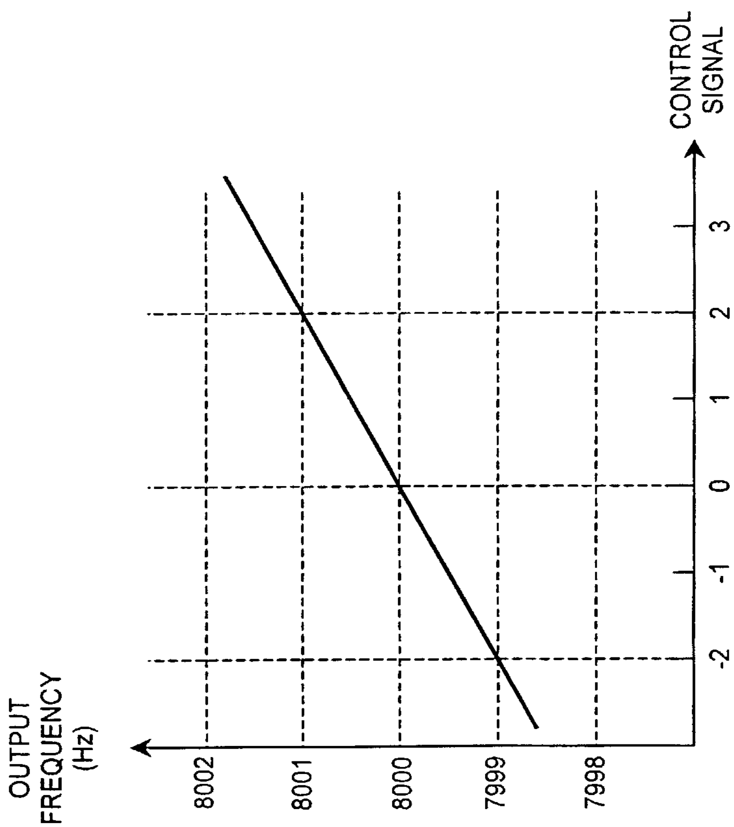
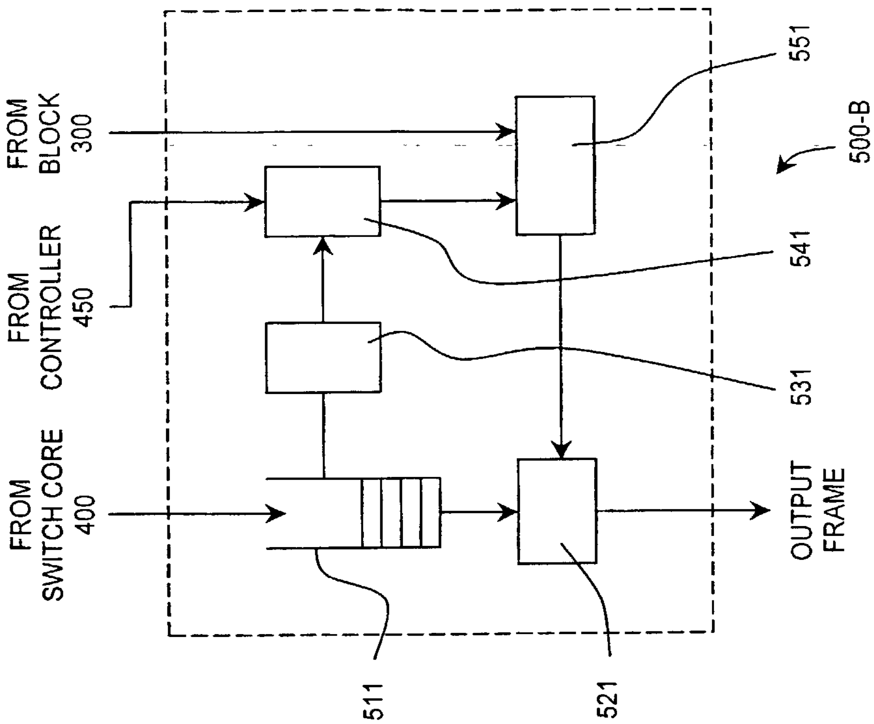

OUTPUT
FREQUENCY
(Hz)
8002
8001
8000
7999
7998
-2
-1
0
1
2
3
CONTROL
SIGNAL

FIG. 4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FROM CONTROLLER 450
FROM BLOCK 300
551
541
531
500-B
511
521
OUTPUT FRAME

FIG. 5B

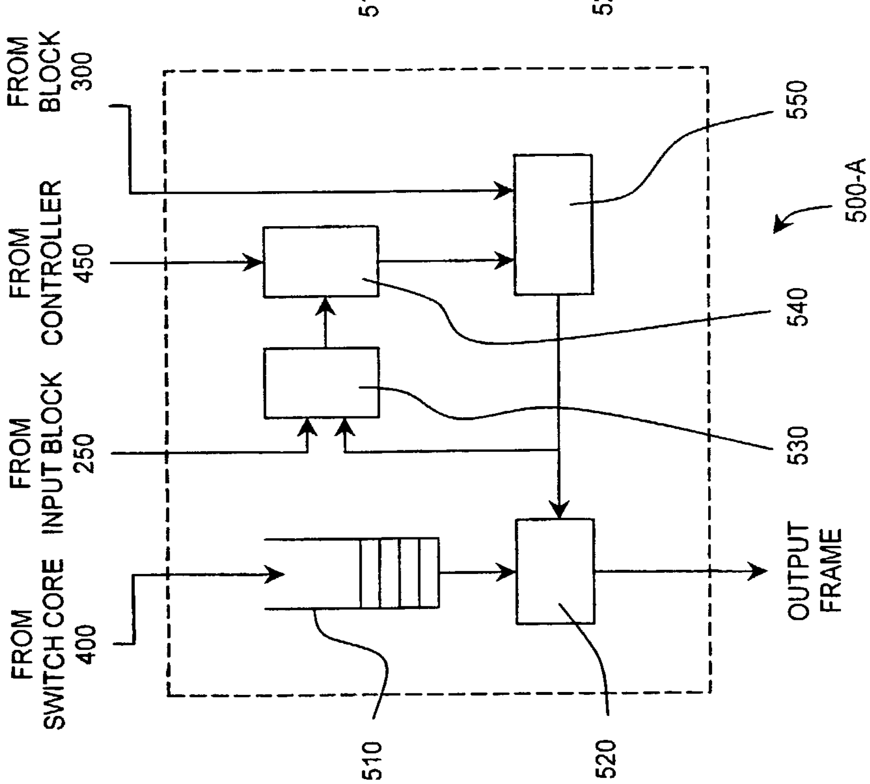
FROM SWITCH CORE 400
FROM INPUT BLOCK 250
FROM CONTROLLER 450
FROM BLOCK 300
550
540
530
500-A
510
520
OUTPUT FRAME

FIG. 5A

#5

DECLARATION FOR NON-PROVISIONAL PATENT APPLICATION*

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below at 201 et seq. beneath my name.

I believe I am the original, first and sole inventor if only one name is listed at 201 below, or an original, first and joint inventor if plural names are listed at 201 et seq. below, of the subject matter which is claimed and for which a patent is sought on the invention entitled

SYNCHRONIZATION METHOD AND APPARATUS

and for which a patent application:
☐ is attached hereto and includes amendment(s) filed on *(if applicable)*
☐ was filed in the United States on as Application No. *(for declaration not accompanying application)*
with amendment(s) filed on *(if applicable)*
☒ was filed as PCT international Application No. PCT/SE00/00873 on May 4, 2000 and was amended under PCT Article 19 on *(if applicable)*

I hereby state that I have reviewed and understand the contents of the above identified application, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

EARLIEST FOREIGN APPLICATION(S), IF ANY, FILED PRIOR TO THE FILING DATE OF THE APPLICATION			
APPLICATION NUMBER	COUNTRY	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
9901654-5	Sweden	6 May 1999	YES ☒ NO ☐
PCT/SE00/00873	PCT	4 May 2000	YES ☒ NO ☐
			YES ☐ NO ☐

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

PROVISIONAL APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

NON-PROVISIONAL APPLICATION SERIAL NO.	FILING DATE	STATUS		
		PATENTED	PENDING	ABANDONED

* for use only when the application is assigned to a company, partnership or other organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

1-00 201	FULL NAME OF INVENTOR	LAST NAME Bohm	FIRST NAME Christer	MIDDLE NAME	
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	POST OFFICE ADDRESS	STREET Skurusundsvägen 40	CITY Nacka	STATE OR COUNTRY Sweden	ZIP CODE SE-131 46
		SIGNATURE OF INVENTOR 201		DATE 20/11 - 2001	
2-00 202	FULL NAME OF INVENTOR	LAST NAME Olsson	FIRST NAME Bengt	MIDDLE NAME J.	
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		SIGNATURE OF INVENTOR 202		DATE 20/11 - 2001	
3-00 203	FULL NAME OF INVENTOR	LAST NAME Danielson	FIRST NAME Magnus	MIDDLE NAME	
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	POST OFFICE ADDRESS	STREET Kyrkvägen 3A	CITY Stocksund	STATE OR COUNTRY Sweden	ZIP CODE SE-182 74
		SIGNATURE OF INVENTOR 203		DATE 20/11 - 2001	
204	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME	
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP	
	POST OFFICE ADDRESS	STREET	CITY	STATE OR COUNTRY	ZIP CODE
		SIGNATURE OF INVENTOR 204		DATE	
205	FULL NAME OF INVENTOR	LAST NAME	FIRST NAME	MIDDLE NAME	
	RESIDENCE & CITIZENSHIP	CITY	STATE OR FOREIGN COUNTRY	COUNTRY OF CITIZENSHIP	
	POST OFFICE ADDRESS	STREET	CITY	STATE OR COUNTRY	ZIP CODE
		SIGNATURE OF INVENTOR 205		DATE	

Rec'd PCT/PTO 21 MAR 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Bohm et al.

Application No.: TBA

Group Art Unit: TBA

Filed: October 22, 2001

Examiner: TBA

For: SYNCHRONIZATION METHOD AND APPARATUS

Attorney Docket No.: 10801-011

POWER OF ATTORNEY BY ASSIGNEE
AND EXCLUSION OF INVENTOR(S) UNDER 37 C.F.R. 3.71

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

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The undersigned assignee of the entire interest in the above-identified subject application hereby appoints: Berj A. Terzian (Reg. No. 20060), David Weild, III (Reg. No. 21094), Jonathan A. Marshall (Reg. No. 24614), Barry D. Rein (Reg. No. 22411), Stanton T. Lawrence, III (Reg. No. 25736), Charles E. McKenney (Reg. No. 22795), Philip T. Shannon (Reg. No. 24278), Francis E. Morris (Reg. No. 24615), Charles E. Miller (Reg. No. 24576), Gidon D. Stern (Reg. No. 27469), John J. Lauter, Jr. (Reg. No. 27814), Brian M. Poissant (Reg. No. 28462), Brian D. Coggio (Reg. No. 27624), Rory J. Radding (Reg. No. 28749), Stephen J. Harbulak (Reg. No. 29166), Donald J. Goodell (Reg. No. 19766), Thomas E. Friebel (Reg. No. 29258), Laura A. Coruzzi (Reg. No. 30742), Jennifer Gordon (Reg. No. 30753), Geraldine F. Baldwin (Reg. No. 31232), Victor N. Balancia (Reg. No. 31231), Samuel B. Abrams (Reg. No. 30605), Steven I. Wallach (Reg. No. 35402), Marcia H. Sundeen (Reg. No. 30893), Paul J. Zegger (Reg. No. 33821), Edmond R. Bannon (Reg. No. 32110), Bruce J. Barker (Reg. No. 33291), Adriane M. Antler (Reg. No. 32605), Thomas G. Rowan (Reg. No. 34419), James G. Markey (Reg. No. 31636), Thomas D. Kohler (Reg. No. 32797), Scott D. Stimpson (Reg. No. 33607), Gary S. Williams (Reg. No. 31066), Ann L. Gisolfi (Reg. No. 31956), Todd A. Wagner (Reg. No. 35399), Scott B. Familant (Reg. No. 35514), Kelly D. Talcott (Reg. No. 39582), Francis D. Cerrito (Reg. No. 38100), Anthony M. Insogna (Reg. No. 35203), Brian M. Rothery (Reg. No. 35340), Brian D. Siff (Reg. No. 35679), Alan Tenenbaum (Reg.

POWER OF ATTORNEY

No. 34939), Michael J. Lyons (Reg. No. 37386), Garland T. Stephens (Reg. No. 37242), William J. Sipio (Reg. No. 34514), Nikolaos C. George (Reg. No. 39201), Stephen S. Rabinowitz (Reg. No. 40286), Ognjan V. Shentov (Reg. No. 38051), and Kenneth L. Stein (Reg. No. 38704), all of Pennie & Edmonds LLP, whose addresses are 1155 Avenue of the Americas, New York, New York 10036, 1667 K Street N.W., Washington, DC 20006 and 3300 Hillview Avenue, Palo Alto, CA 94304, all of Pennie & Edmonds LLP (PTO Customer No. 20583), as its attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, said appointment to be to the exclusion of the inventors and their attorney(s) in accordance with the provisions of 37 C.F.R. 3.71, provided that, if any one of these attorneys ceases being affiliated with the law firm of Pennie & Edmonds LLP as partner, counsel, or employee, then the appointment of that attorney and all powers derived therefrom shall terminate on the date such attorney ceases being so affiliated.

An assignment of the entire interest in the above-identified subject application:

[ ] was recorded on ________________ at reel/frame _/______.

[ ] is submitted herewith for recording.

[x] A copy of an assignment of the entire interest in the above-identified subject application is submitted herewith. The assignment will be duly recorded.

Please direct all correspondence for this application to customer no. 20583.

ASSIGNEE: NET INSIGHT AB

Signature: ________________

Typed Name: TOMAS DUFFY

Position/Title: CEO

Address: BOX 42093
SE-126 14 STOCKHOLM
SWEDEN

Date: December 7, 2001

NY2 - 1249129.1

JOINT

ASSIGNMENT

WHEREAS, WE, Christer Bohm, Bengt J. Olsson, and Magnus Danielson, ASSIGNORS, citizens of Sweden, residing at Skurusundsvägen 40, SE-131 46 Nacka, Sweden, Rådjursvägen 303, SE-147 34 Tumba, Sweden, and Kyrkvägen 3A, SE-182 74 Stocksund, Sweden, respectively, are the inventors of the invention in SYNCHRONIZATION METHOD AND APPARATUS for which we have executed an application for a Patent of the United States

☒ which is identified by Pennie & Edmonds LLP docket no. 10806-011
☒ which was filed on October 22, 2001, Application No. TBA

and WHEREAS, Net Insight AB, ASSIGNEE, a corporation organized under the laws of Sweden, is desirous of obtaining our entire right, title and interest in, to and under the said invention and the said application:

NOW, THEREFORE, in consideration of the sum of One Dollar ($1.00) to us in hand paid, and other good and valuable consideration, the receipt of which is hereby acknowledged, we, the said ASSIGNORS, have sold, assigned, transferred and set over, and by these presents do hereby sell, assign, transfer and set over, unto the said ASSIGNEE, its successors, legal representatives and assigns, our entire right, title and interest in, to and under the said invention, and the said United States application and all divisions, renewals and continuations thereof, and all Patents of the United States which may be granted thereon and all reissues and extensions thereof; and all applications for industrial property protection, including, without limitation, all applications for patents, utility models, and designs which may hereafter be filed for said invention in any country or countries foreign to the United States, together with the right to file such applications and the right to claim for the same the priority rights derived from said United States application under the Patent Laws of the United States, the International Convention for the Protection of Industrial Property, or any other international agreement or the domestic laws of the country in which any such application is filed, as may be applicable; and all forms of industrial property protection, including, without limitation, patents, utility models, inventors' certificates and designs which may be granted for said invention in any country or countries foreign to the United States and all extensions, renewals and reissues thereof;

AND WE HEREBY authorize and request the Commissioner of Patents and Trademarks of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents or other evidence or forms of industrial property protection on applications as aforesaid, to issue the same to the said ASSIGNEE, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND WE HEREBY covenant and agree that we have full right to convey the entire interest herein assigned, and that we have not executed, and will not execute, any agreement in conflict herewith.

AND WE HEREBY further covenant and agree that we will communicate to the said ASSIGNEE, its successors, legal representatives and assigns, any facts known to us respecting said invention, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing, reissue and foreign applications, make all rightful oaths, and generally do everything possible to aid the said ASSIGNEE, its successors, legal representatives and assigns, to obtain and enforce proper protection for said invention in all countries.

IN TESTIMONY WHEREOF, We hereunto set our hands and seals the day and year set opposite our respective signatures.

Date 20/11 - 2001, 2001 ______________________ L.S.
Christer Bohm (Signature)

On this 20 day of November, 2001, before me, a witness, personally appeared Christer Bohm, to me known and known to me to be the person of that name, who signed the foregoing instrument, and he acknowledged the same to be his free act and deed.

______________________ Witness

Date 20/11 - 2001, 2001 Bengt J. Olsson L.S.
Bengt J. Olsson (Signature)

On this 20 day of November, 2001, before me, a witness, personally appeared Bengt J. Olsson, to me known and known to me to be the person of that name, who signed the foregoing instrument, and he acknowledged the same to be his free act and deed.

______________________ Witness

Date 20/11 - 2001, 2001 ______________________ L.S.
Magnus Danielson (Signature)

On this 20 day of November, 2001, before me, a witness, personally appeared Magnus Danielson, to me known and known to me to be the person of that name, who signed the foregoing instrument, and he acknowledged the same to be his free act and deed.

Sten Björnevro
______________________ Witness